NetFPGA SUME: Toward Commodity 100Gb/s

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***Abstract*—The demand-led growth of datacenter networks has meant that many constituent technologies are beyond the budget of the wider community. In order to make and validate timely and relevant new contributions, the wider community requires accessible evaluation, experimentation and demonstration environments with specification comparable to the subsystems of the most massive datacenter networks. We will demonstrate NetFPGA SUME, an open-source FPGA-based PCIe board with I/O capabilities for 100Gbps operation as NIC, multiport switch, firewall, or test/measurement environment.**

I. The NetFPGA project

The NetFPGA project (http://www.netfpga.org) provides software, hardware and community as a basic infrastructure to simplify design, simulation and testing, all around an open-source high-speed networking platform. Beyond the hardware and software, the NetFPGA project is backed by community resources that include online forums, tutorials, summer camp events and developer workshops all supported by the NetFPGA project team. As all the (reference) projects developed under the NetFPGA project are open-source, by reusing building blocks across projects users compare design utilization and performance. Reference projects, included in all NetFPGA distributions, are a NIC, a switch and an IPv4 router.

II. NetFPGA SUME

The NetFPGA SUME design aims to create a low-cost, PCIe host adapter card able to support 40Gb/s and 100Gb/s applications. At the core of the board is a Xilinx Virtex-7 690T FPGA device. There are five peripheral subsystems that complement the FPGA. A high-speed serial interfaces subsystem composed of 30 serial links running at up to 13.1Gb/s. These connect four 10Gb/s SFP+ Ethernet interfaces, two expansion connectors and a PCIe edge connector directly to the FPGA. The second subsystem, the latest generation 3.0 of PCIe is used to interface between the card and the host device, allowing both register access and packet transfer between the platform and the motherboard. The memory subsystem combines both SRAM and DRAM devices. SRAM memory is devised from three 36-bit QDRII+ devices, running at 500MHz. The DRAM memory is composed of two 64-bit DDR3 memory modules running at 933MHz (1866MT/s). Storage subsystems of the design permit both a MicroSD card and external disks through two SATA interfaces. Finally, the FPGA configuration subsystem is concerned with use of the FLASH devices. Additional NetFPGA SUME features support debug, extension and synchronization of the board. The board is implemented as a dual-slot, full-size PCIe adapter, that can operate as a standalone unit outside of a PCIe host. It is manufactured by Digilent Inc.(http://www.digilentinc.com).

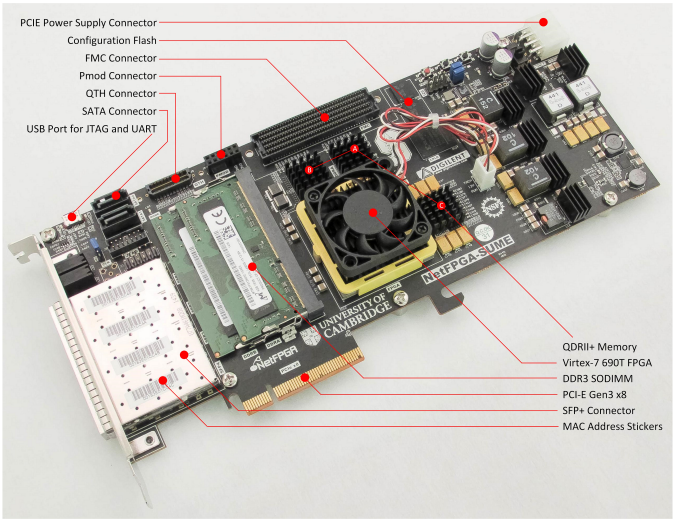

Fig. 1. NetFPGA SUME Board

III. Demonstration

We present the NetFPGA SUME platform, the NetFPGA development environment and a reference application exercising all of NetFPGA SUME interfaces. We show the development flow over the platform: code development, simulation environment and test harness. Our project also provides access to an open-source code repository, online documentation and user forums, and debug tools. We provide a glimpse into the use of these tools under the demonstrated application, showing the performance of the hardware.

Acknowledgements

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